dh

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,340	01/22/2004	Yen-Chang Chiu	MR2707-57	3276

4586 7590 05/05/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
NGUYEN, TUAN HOANG	
ART UNIT	**PAPER NUMBER**
2618	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,340	CHIU ET AL.	
	Examiner	Art Unit	
	Tuan H. Nguyen	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 14-15, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al. (U.S PUB. 2003/0058961 hereinafter "Fling") in view of Le Torc'h (U.S PAT. 6,483,827).

Regarding claim 1, Fling discloses a single crystal oscillator RF transmitter system comprising: a microprocessor (page 4 [0051]); a local oscillator responsive to an external crystal for generating a first clock (Fig. 15 page 12 [0137]); a clock switch, connected with the first clock, for providing a second clock to the microprocessor and a

third clock to the converter (Fig. 15 page 12 [0137]); and a transmitter connected with the first clock and RF packets for generating an RF signal to be sent out (Fig. 15 page 13 [0140]). Fling differs from the claimed invention in not specifically teaching a converter for converting a data to be transmitted into RF packets. However, Le Torc'h teaches a converter (item 10) for converting a data to be transmitted into RF packets (Fig. 2 col. 4 lines 1-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Fling for a converter for converting a data to be transmitted into RF packets, as per teaching of Le Torc'h, because it provides the DECT ("Digital Enhanced Cordless Telecommunications") frame is modified in order to lower the bit rate of the modulating signal and hence the spectral bandwidth of the transmitted radio signal.

Regarding claim 2, Fling further discloses the clock switch comprises a frequency divider for frequency-dividing the first clock to generate the second clock (Fig. 15 page 12 [0137]).

Regarding claim 3, Fling further discloses the clock switch comprises a frequency divider for frequency-dividing the first clock to generate the third clock (Fig. 15 page 12 [0137]).

Regarding claim 14, Fling discloses a method for transmitting a data by sending out an RF signal by a single crystal oscillator RF transmitter system including a

microprocessor connected with a converter that is further connected to a transmitter (page 4 [0051]), the method comprising the steps of: generating a first clock responsive to the single crystal oscillator for providing to the transmitter (Fig. 15 page 12 [0137]); generating a second clock and a third clock from the first clock for providing to the microprocessor and converter, respectively (Fig. 15 page 12 [0137]); and generating the RF signal from the RF packets and sending out the RF signal by the transmitter (Fig. 15 page 13 [0140]). Fling differs from the claimed invention in not specifically teaching converting the data into RF packets by the converter for providing to the transmitter. However, Le Torc'h teaches converting the data into RF packets by the converter for providing to the transmitter (Fig. 2 col. 4 lines 1-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Fling for converting the data into RF packets by the converter for providing to the transmitter, as per teaching of Le Torc'h, because it provides the DECT ("Digital Enhanced Cordless Telecommunications") frame is modified in order to lower the bit rate of the modulating signal and hence the spectral bandwidth of the transmitted radio signal.

Regarding claim 15, Fling further discloses the step of generating a second clock and a third clock from the first clock comprises the step of frequency-dividing the first clock (Fig. 15 page 12 [0137]).

Regarding claim 16, Fling discloses a method for transmitting a data by sending out an RF signal by a single crystal oscillator RF transmitter system including a microprocessor connected with a converter that is further connected to a transmitter (page 4 [0051]), the method comprising the steps of: generating a first clock by an RC oscillator (Fig. 15 page 12 [0137]); generating a second clock from the first clock for providing to the microprocessor (Fig. 15 page 12 [0137]); generating a third clock responsive to the single crystal oscillator (Fig. 15 page 12 [0137]); generating a fourth clock from the third clock for providing to the converter (Fig. 15 page 12 [0137]); and receiving the RF packets and the first clock by the transmitter at which to generate the RF signal send out (Fig. 15 page 13 [0140]). Fling differs from the claimed invention in not specifically teaching converting the data into RF packets by the converter. However, Le Torc'h teaches converting the data into RF packets by the converter (Fig. 2 col. 4 lines 1-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Fling for converting the data into RF packets by the converter, as per teaching of Le Torc'h, because it provides the DECT ("Digital Enhanced Cordless Telecommunications") frame is modified in order to lower the bit rate of the modulating signal and hence the spectral bandwidth of the transmitted radio signal.

Regarding claim 17, Fling further discloses the step of generating a fourth clock from the third clock comprises the step of frequency-dividing the third clock (Fig. 15

page 12 [0137]).

4. Claims 4-7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al. (U.S PUB. 2003/0058961 hereinafter "Fling") in view of Le Torc'h (U.S PAT. 6,483,827) as applied to claims above, and further in view of Tian (U.S PAT. 6,624,710).

Regarding claim 4, Fling and Le Torc'h, in combination, fails to discloses an RC oscillator for generating the second clock. However, Tian teaches an RC oscillator for generating the second clock (col. 1 lines 26-37). Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Tian into view of Fling and Le Torc'h, in order to provide frequency of the output signal generated by the oscillator output signal is set as a function of a value of an included internal resistor integrated on the chip. An external resistor may be connected to the chip to allow a user to manipulate the oscillator output signal frequency.

Regarding claim 5, Fling further discloses the clock switch comprises a frequency divider for frequency-dividing the first clock to generate the third clock (Fig. 15 page 12 [0137]).

Regarding claim 6, Tian further discloses the RC oscillator is connected with an external resistor for tuning the second clock (col. 1 lines 26-37).

Regarding claim 7, Tian further discloses the external resistor comprises a variable resistor (col. 2 line 66 through col. 3 line 7).

Regarding claim 18, Tian further discloses the step of tuning an external resistor connected to the RC oscillator for determining the first clock (col. 1 lines 26-37).

5. Claims 11-12 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al. (U.S PUB. 2003/0058961 hereinafter "Fling") in view of Le Torc'h (U.S PAT. 6,483,827) as applied to claims above, and further in view of Yamazaki et al. (U.S PAT. 5,398,007 hereinafter "Yamazaki").

Regarding claim 11, Fling and Le Torc'h, in combination, fails to discloses a peripheral circuit connected to the microprocessor. However, Yamazaki teaches a peripheral circuit connected to the microprocessor (col. 7 lines 1-6). Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Yamazaki into view of Fling and Le Torc'h, in order to generate accurate baud rates for serial communication in a microcontroller running at a low system clock frequency, without restricting communication to low baud rates, drawing extra current and power, or requiring an extra external resonator.

Regarding claim 12, Yamazaki further discloses the microprocessor, converter, local oscillator, clock switch and transmitter are integrated on a chip (col. 7 lines 1-6).

Regarding claim 19, Yamazaki further discloses the step of trimming a built-in resistor network connected to the RC oscillator for determining the first clock (col. 5 lines 49-59).

Regarding claim 20, Yamazaki further discloses the step of signaling the single crystal oscillator to stop generating the third clock after sending out the RF signal (col. 5 lines 15-19).

Regarding claim 21, Yamazaki further discloses the step of signaling the converter to turn off after sending out the RF signal (col. 7 lines 1-6).

Regarding claim 22, Yamazaki further discloses the step of signaling the transmitter to turn off after sending out the RF signal (col. 7 lines 1-6).

6. Claims 8-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al. (U.S PUB. 2003/0058961 hereinafter "Fling") in view of Le Torc'h (U.S PAT. 6,483,827) and Tian (U.S PAT. 6,624,710) as applied to claims above, and further in view of Yamazaki et al. (U.S PAT. 5,398,007 hereinafter "Yamazaki").

Regarding claim 8, Fling, Le Torc'h, and Tian, in combination, fails to discloses the RC oscillator comprises a resistor network for determining the second clock. However, Yamazaki teaches the RC oscillator comprises a resistor network for determining the second clock (Fig. 6 col. 5 lines 49-59). Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Yamazaki into view of Fling, Le Torc'h, and Tian, in order to generate accurate baud rates for serial communication in a microcontroller running at a low system clock frequency, without restricting communication to low baud rates, drawing extra current and power, or requiring an extra external resonator.

Regarding claim 9, Yamazaki further discloses the microprocessor signals the local oscillator to turn off after the RF signal is sent out (col. 5 lines 15-19).

Regarding claim 10, Yamazaki further discloses the converter and transmitter signal the local oscillator to turn off after the RF signal is sent out (col. 7 lines 1-6).

Regarding claim 13, Yamazaki further discloses the microprocessor, converter, local oscillator, clock switch, RC oscillator and transmitter are integrated on a chip (col. 7 lines 1-6 and col. 2 line 45 through col. 3 line 20).

Conclusion

7. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571) 272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen
Examiner
Art Unit 2618

NAY MAUNG
SUPERVISORY PATENT EXAMINER